21.3 A 100Hz 5nT/√Hz Low-Pass ΔΣ Servo-Controlled Microfluxgate Magnetometer Using Pulsed Excitation

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Integrated microfluxgate sensors [1] are considered to be today's most sensitive magnetic field microsensors operating at room temperature. They exhibit low noise and low temperature sensitivity, which makes them suitable for applications such as portable compasses, current sensors and magnetic ink reading. Recently, research efforts have been undertaken to fully integrate the readout interface, especially the sensor's output A/D conversion [2]. However, most devices still use an analog phase-sensitive demodulation readout interface [3]. The drawback of the analog output is that tremendous efforts have to be made on the analog closed-loop design, leading to increased complexity and power. The circuit presented in this paper reduces the complexity by using a programmable digital closed-loop, which benefits from a high-resolution ΔΣ conversion. One major advantage of this scheme is that the sensor is embedded in the digital loop, so that the proposed architecture can easily be adjusted for different applications.

Figure 21.3.1 shows the system architecture. The sensing operation is performed as follows: the drive coil is excited using short voltage pulses; on the pickup coil, the magnitude of the resulting voltage is proportional to the external magnetic field and increases with the slope of the excitation pulses. This measurement technique [4] enables a low-pass readout, performed by a 2nd-order ΔΣ modulator. In the open-loop operating mode, the ΔΣ modulator output represents the magnetic field. When the sensor is exposed to large fields, distortion appears due to non-linearities. To enhance the system dynamics, the sensor is inserted in a digital closed-loop structure so that a built-in magnetic field injected in the pickup coil cancels out the external magnetic field. This feedback field is produced from the ΔΣ output through a compensation filter which drives a FIR-DAC current generator.

Figure 21.3.2 shows how the pickup signal is sampled at the front-end of the switched-capacitor ΔΣ modulator. Since the pickup signal can be very narrow in time (20ns), the settling time to charge the sampling capacitor C_a has to be as small as possible; that is, the input switch R_{on} and C_a must be small. Making R_{on} and C_a small, however, results in large charge injection and significant thermal noise. To circumvent this issue, the pickup signal width is increased using a "box-car" averager [5] modified as follows: the pickup signal is sampled through several successive occurrences during phase phi1. The charge transfer occurs during phase phi2. Furthermore, in order to compensate the parasitic offset caused by the feedback current flowing through the pickup coil, the sampling capacitor C_a is connected to the signal lines during phase phi2 (Fig. 21.3.2). Therefore only the differential voltage between phi1 and phi2 is detected.

The ΔΣ modulator is fully differential, with two integrator stages, and a single feedback loop in the first stage [6]. The ΔΣ 1b output drives a digital compensation filter. It is a 2nd-order ΔΣ-IIR filter [7], where the signal is modulated to a 1b format at every node of the lattice. This helps to save some valuable circuit size, because multi-bit multiplications are replaced by simple 2-input multiplexers. The 32b fixed-point filter coefficients are programmable, which facilitates the circuit adaptating to sensor behavior and the mapping of the device to different applications.

At this point, the 1b output of the compensation filter contains high-frequency quantization noise due to ΔΣ noise shaping, which can drastically reduce the system linearity because the feedback field does not compensate for the external field. To solve this problem, the 1b feedback signal feeds a low-pass FIR-DAC [8], simultaneously performing 1b D/A conversion, low-pass filtering and current driving into the pickup coil (Fig. 21.3.3). The FIR-DAC in its current mode version is made with a delay line where at each node a current source is driven according to the one-bit signal: when this signal is 1 (0), a positive (negative) current is injected into the sensor. The value of the current source at each node represents the FIR coefficient. To simplify the implementation, a 15th-order sinc filter is chosen, the transfer function of which can be expressed as

$$\mathrm{FIR}(z^{-1}) = \alpha \sum_{i=0}^{14} n_i z^{-i}, n_i \in N,$$

where α is the value of the unit current source and the n_i are integer numbers that represent the number of unit current sources placed in parallel. Such an implementation enhances the FIR linearity since the same current source is always used. Special care has been taken in the layout to reduce mismatch between unit sources: each unit source is divided into two half cells, positioned according to a central symmetry in order to compensate 1st-order gradient effects.

The digital part of the circuit is clocked at a sampling frequency of 50kHz, while the master clock is 50MHz. Therefore, the oversampling ratio is 250 for a 100Hz bandwidth. The digital is configured via a standard SPI link. The circuit allows the sensor to be used in either an open-loop or a closed-loop mode. The dynamics of the ΔΣ modulator can be programmed by using different feedback capacitors, and the closed-loop dynamics are set by the adjustable FIR-DAC driver-unit current. The compensation filter is a proportional-plus-integral controller whose gain is adjusted to avoid saturating the internal digital ΔΣ loop.

In open-loop operation, the measured sensor intrinsic sensitivity is 172V/T, while the noise floor is 3.5nT/√Hz in the 1 to 100Hz range, which corresponds to the intrinsic measured sensor's noise. The microfluxgate sensor's linear range is, however, intrinsically limited to fields below 10μT and distortion appears when large fields are applied; Fig. 21.3.4 shows the PSD of the ΔΣ modulator output in open-loop operation when a field of 64μT is applied. Closed-loop operation makes it possible to enhance the linear range of the system, as shown in Fig. 21.3.5. In that configuration, the noise floor is 3.4nT/√Hz in the 1 to 100Hz range. The peak SNDR over a 120μT dynamic range is 60dB.

The circuit draws 8.3mA from a 3.3V supply when operating open-loop and 11mA in closed-loop operation. Most of the power consumption (6mA) comes from the sensor excitation, a 500kHz burst of 40ns pulses at 3.3V. The digital part dissipates 1.3mA. The FIR-DAC draws 2.7mA for full-scale operation in closed-loop. Figure 21.3.6 summarizes the overall performance. The chip (Fig. 21.3.7) was fabricated using a 0.35μm CMOS technology. Its area is 9mm².

The circuit presented in this paper shows improves on the state of the art [9], in regard to noise level in both open- and closed-loop modes, and has greater distortion rejection over a larger DR. It should be noted that the system's resolution is not limited by the ASIC and that it can be improved by reducing the intrinsic sensor's noise. Further progress can be achieved by adjusting the compensation filter using pre-identification of the sensor transfer function and control theory. The focal point of this system is its adaptability to a given application; of special importance are the facts that the sensor driving and sampling frequency can be adjusted to the required resolution, power consumption, BW and/or DR.

References:

[1] P. Ripka, "Advances in Fluxgate Sensors," *Sensors and Actuators A: Physical*, pp. 8-14, 2003.
[2] S. Kawahito et al., "A Weak Magnetic Field Measurement System Using Micro-Fluxgate Sensors and Delta-Sigma Interface," *IEEE T. Instr. and Meas.*, Feb., 2003.
[3] A. Baschirotto et al., "A CMOS Front-End Circuit for Integrated Fluxgate Magnetic Sensors," *ISCAS Proc.,* pp. 4403-4406, 2006.
[4] Patent FR_0650280, "Méthode d'excitation Pulsée et de Détection Associée pour Capteur Fluxgate," [Pulsed Excitation and Related Detection Method for Fluxgate Sensor]
[5] K. Neelakantan, "Signal-to-Noise Enhancement Using Delta Modulation," *J. Physics E: Scientific Instruments*, Vol. 16, pp 278-282, April, 1983.
[6] B. Wang et al., "New High-Precision Circuits for On-Chip Capacitor Ratio Testing and Sensor Readout," *ISCAS Proc.*, Vol. 1, pp. 547-550, 1998.
[7] D.A. Johns and D.M. Lewis, "IIR Filtering on Sigma-Delta Modulated Signals," *IEE Electronics Letters,* Vol. 27, Issue 4, pp. 307-308, 1991.
[8] D.K. Su and B.A. Wooley, "A CMOS Oversampling D/A Converter with a Current-Mode Semidigital Reconstruction Filter," *IEEE J. Solid-State Circuits*, pp. 1224-1233, Dec., 1993.
[9] P. Drljaca et al., "Low-Power 2-D Fully Integrated CMOS Fluxgate Magnetometer," *IEEE Sensors Journal*, Vol. 5, Issue 5, pp. 909-915, Oct., 2005.

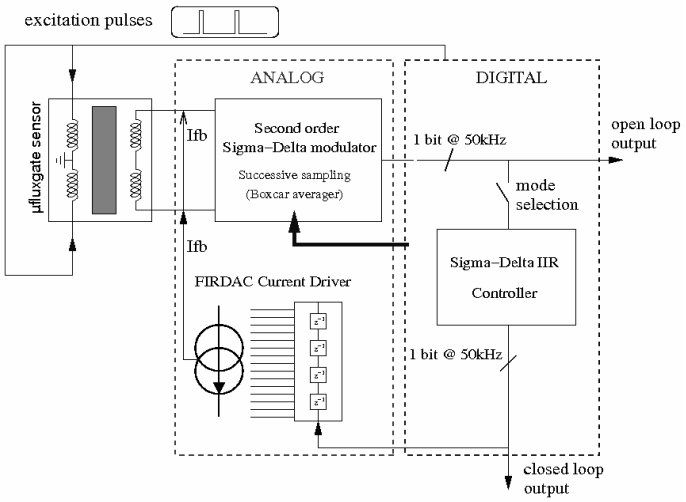

Figure 21.3.1: ASIC system overview.

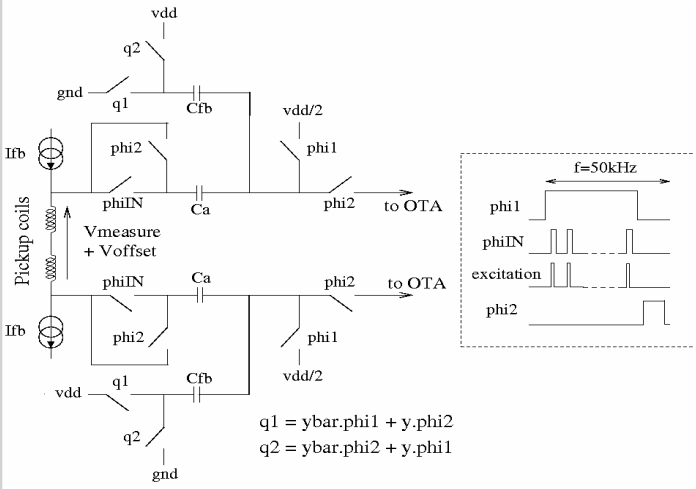

Figure 21.3.2: ΔΣ first stage and phase timing diagram.

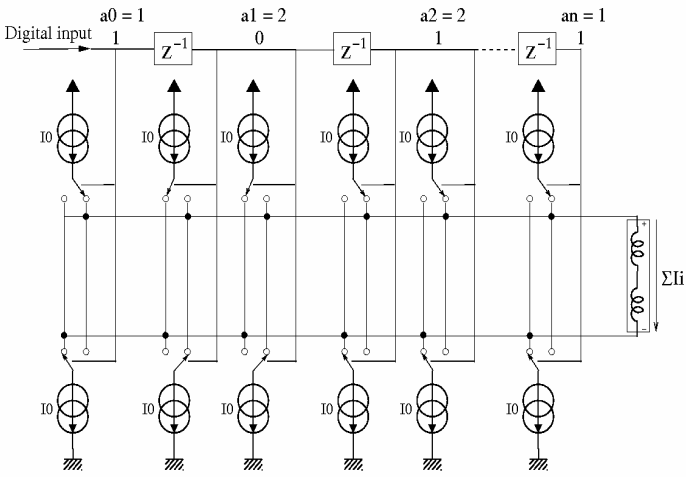

Figure 21.3.3: FIR-DAC current driver.

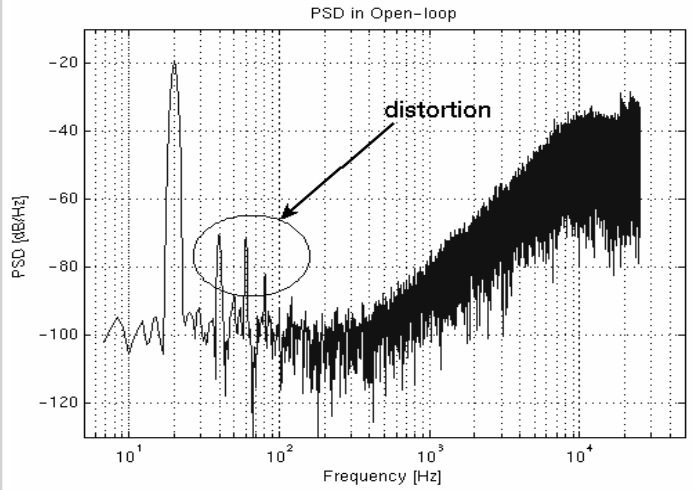

Figure 21.3.4: PSD of the system output in open loop operation when a 64µT @ 20Hz external field is applied.

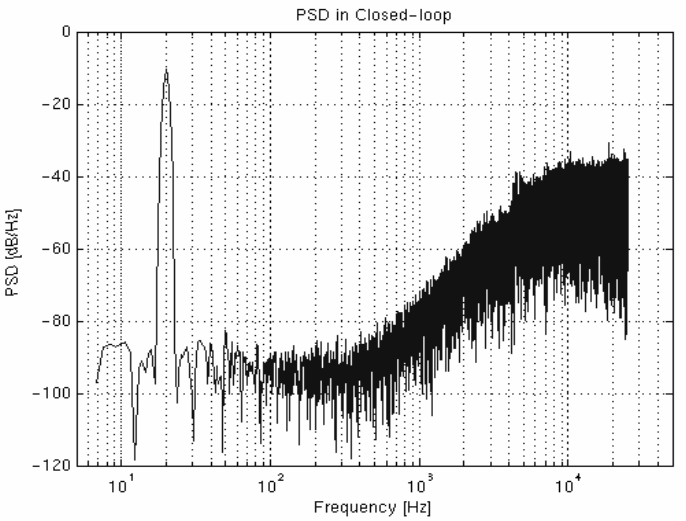

Figure 21.3.5: PSD of the system output in closed-loop operation when a 64µT @ 20Hz external field is applied.

	State of the art [9]	This paper
Sensor intrinsic sensitivity	92,5 V/T	172 V/T
Dynamic range	60µT	120µT
Bandwidth (Hz)	10	100
Closed-loop peak SNDR	-	60dB
Noise PSD @1Hz	15 nT/√Hz	5 nT/√Hz
Power (mW)	10	36

Figure 21.3.6: Microsystem performance compared to state of the art.

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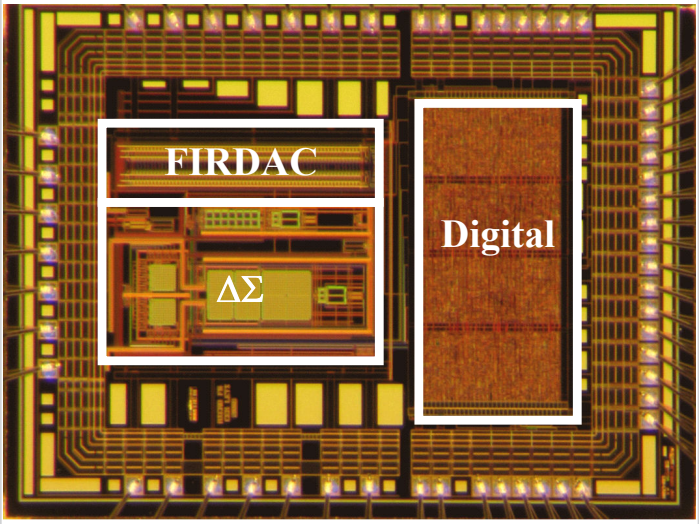

Figure 21.3.7: Die micrograph (9mm²).

